UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/809,908 | 03/26/2004 | Susie Xiuru Yang | 008066<br>USA/MTCG/PCTRL/JW | 7263 |

7590 11/23/2005

Applied Materials, Inc.
P.O. Box 450A
Santa Clara, CA 95052

| EXAMINER | |
|---|---|
| JARRETT, RYAN A | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2125 | |

DATE MAILED: 11/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/809,908 | YANG ET AL. | |
| | Examiner | Art Unit | |
| | Ryan A. Jarrett | 2125 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to the have been considered but are moot in view of the new ground(s) of rejection. The Applicant's amendments have been addressed in the body of the rejection below.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7-15, 17-25, and 27-30 are under 35 U.S.C. 103(a) as obvious over Chen et al. US 6,756,309 in view of Sonderman et al. US 6,751,518. Applicant's claims are directed towards a "computer-implemented method", a "computer-assisted system", and "a computer program having instructions stored on a computer-readable medium". Chen et al. discloses most all the steps and functional limitations of the aforementioned claims, but does not *explicitly* disclose the use of a "computer" or a "controller" or a "computer program" to carry out the steps. Such a teaching is clearly implied by the disclosure of Chen et al. Taking claim 1 as an example, Chen et al. implies that the data-collection steps (A), (B), and (C) are computer-implemented since Chen et al.

discloses various metrology tools and methods used to collect the layer thickness data and the trench profile data, such as variable angle spectroscopic ellipsometry, reflection spectroscopy, FTIR spectroscopy, X-ray fluorescence, and scanning electron microscopes (e.g., col. 3 lines 15-25, col. 4 lines 1-4). These data collection methods and tools require the use of a computer. Chen et al. also implies that steps (C) and (D) are computer-implemented since Chen et al. discloses that layer thickness and trench depth dimensions are "fed-forward" to be used in determining a targeted metal line thickness (col. 5 lines 1-4), and since Chen et al. discloses "projecting" new polishing endpoints (CMP time period) in order to achieve the targeted metal line thickness. Terms such as "feed-forward" and "project" imply the use of a computer, in the context of Chen's disclosure.

Alternatively, it additionally would have been obvious to one having ordinary skill in the art at the time the invention was made to use a computer to carry out the method of Chen et al. in order to increase throughput by automating the process and to eliminate the potential for human error, and since it is well known to use computers in semiconductor feed-forward and feed-back process control systems.

Regarding claims 1-2, 5, 7, 11, 12, 15, 17, 21-23, 25, and 27,

Chen et al. discloses:

1. A computer-implemented method for controlling metal line resistance (RS) uniformity in a semiconductor manufacturing process using integrated or in-line metrology, comprising the steps of:

(A) collecting first data representative of at least one measurement of a first thickness of at least one deposition layer, subsequent to a deposition process on at least one semiconductor product (e.g., Fig. 2B #A1, col. 3 lines 15-61);

(B) collecting second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one deposition layer, subsequent to an etch process on the at least one semiconductor product (e.g., Fig. 2B #C1, Fig. 2B #B2, col. 3 line 62 – col. 4 line 23);

(C) collecting third data representative of at least one measurement of a second thickness of the at least one deposition layer (e.g., Fig. 2D #A2, col. 5 lines 36-48), and a thickness of a metal deposited in the at least one trench (e.g., Fig. 2D #B3, col. 5 lines 36-48), on the at least one semiconductor product;

(D) determining an area of a cross section of metal in the at least one trench at the profile and comparing the resistance of the area to a target resistance (e.g., col. 4 lines 40-60); and

(E) determining a planarization process to adjust an amount of metal in the at least one trench to approximate the target resistance in the at least one semiconductor product (e.g., col. 5 lines 10-54).

2. The method of claim 1, further comprising utilizing the determined planarization process for at least one of: the at least one semiconductor product (e.g., col. 5 lines 10-54), another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product.

5. The method of claim 1, wherein the at least one deposition layer includes a dielectric deposition layer, and wherein the deposition process is a chemical vapor deposition process (e.g., col. 3 lines 35-45).

7. The method of claim 1, wherein the third data includes data representative of a measurement of the amount of dishing and/or erosion of the method in the at least one trench (e.g. col. 5 lines 52-54, *EN: Sonderman et al. takes into account the amount of metal dishing to determine the targeted metal line thickness. For an "amount of metal dishing" to be determined or taken into account, it*

*is inherent that some sort of "measurement" takes place. There is no other way for the amount of metal dishing be determined or taken into account.*).

11. A computer-assisted system for controlling metal line resistance (RS) uniformity, in a semiconductor manufacturing process using integrated or in-line metrology components, comprising:

(A) at least one first component, to collect first data representative of at least one measurement of a first thickness of at least one deposition layer, subsequent to a deposition process on at least one semiconductor product (e.g., Fig. 2B #A1, col. 3 lines 15-61);

(B) at least one second component, to collect second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one deposition layer, subsequent to an etch process on the at least one semiconductor product (e.g., Fig. 2B #C1, Fig. 2B #B2, col. 3 line 62 – col. 4 line 23);

(C) at least one third component, to collect third data representative of at least one measurement of a second thickness of the at least one deposition layer (e.g., Fig. 2D #A2, col. 5 lines 36-48), and a thickness of a metal deposited in the at least one trench, on the at least one semiconductor product (e.g., Fig. 2D #B3, col. 5 lines 36-48); and

(D) at least one controller, communicating with the at least one first component, the at least one second component, and the at least one third component, to determine an area of a cross section of metal in the at least one trench at the profile, and to compare the resistance of the area to a target resistance (e.g., col. 4 lines 40-60); and to determine a planarization process, so as to leave an amount of metal in the at least one trench, approximating the target resistance in the at least one semiconductor product (e.g., col. 5 lines 10-54).

12. The system of claim 11, wherein the at least one controller utilizes the determined planarization process for at least one of: the at least one semiconductor product (e.g., col. 5 lines 10-54), another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product.

15. The system of claim 11, wherein the at least one deposition layer includes a dielectric deposition layer, and wherein the deposition process is a chemical vapor deposition process (e.g., col. 3 lines 35-45).

17. The system of claim 11, wherein the third data includes data representative of a dishing and/or erosion of the method in the at least one trench (e.g. col. 5 lines 52-54).

21. A computer program for controlling metal line resistance (RS) uniformity, in a semiconductor manufacturing process using integrated or in-line metrology, the computer program having instructions stored on at least one computer-readable medium, comprising:

(A) instructions for collecting first data representative of at least one measurement of a first thickness of at least one deposition layer, subsequent to a deposition process on at least one semiconductor product (e.g., Fig. 2B #A1, col. 3 lines 15-61);

(B) instructions for collecting second data representative of a plurality of measurements characterizing a profile of at least one trench in the at least one deposition layer, subsequent to an etch process on the at least one semiconductor product (e.g., Fig. 2B #C1, Fig. 2B #B2, col. 3 line 62 – col. 4 line 23);

(C) instructions for collecting third data representative of at least one measurement of a second thickness of the at least one deposition layer (e.g., Fig. 2D #A2, col. 5 lines 36-48), and a thickness of a metal deposited in the at least one trench (e.g., Fig. 2D #B3, col. 5 lines 36-48), on the at least one semiconductor product;

(D) instructions, on the computer-readable medium, for determining an area of a cross section of metal in the at least one trench at the profile and for comparing the resistance of the area to a target resistance (e.g., col. 4 lines 40-60); and

(E) instructions for determining a planarization process, so as to leave an amount of metal in the at least one trench, approximating the target resistance in the at least one semiconductor product (e.g., col. 5 lines 10-54).

22. The computer program of claim 21, further comprising instructions for utilizing the determined planarization process for at least one of: the at least one semiconductor product (e.g., col. 5

lines 10-54), another semiconductor product subsequent to the at least one semiconductor product, a lot of semiconductor products including the at least one semiconductor product, and a lot of semiconductor products including the other semiconductor product.

23. The computer program of claim 21, further comprising instructions for utilizing at least one of: the second data to adjust a lithography process and/or the etch process, and the third data to adjust the planarization process (e.g., col. 5 lines 10-54), for another semiconductor product subsequent to the at least one semiconductor product.

25. The computer program of claim 21, wherein the at least one deposition layer includes a dielectric deposition layer, and wherein the deposition process is a chemical vapor deposition process (e.g., col. 3 lines 35-45).

27. The computer program of claim 21, wherein the third data includes data representative of a dishing and/or erosion of the method in the at least one trench (e.g. col. 5 lines 52-54).

Regarding independent claims 1, 10, 11, 20, 21, and 30, Chen et al. fails to explicitly disclose adjusting the deposition process based on a comparison of the first data with data representative of a target deposition layer thickness, the target deposition layer thickness being determined prior to the collection of the first data.

Sonderman et al. discloses adjusting a deposition process based on a comparison of a first thickness measurement data with data representative of a target deposition layer thickness, the target deposition layer thickness being determined prior to the collection of the first data (e.g., col. 7 lines 30-40, col. 6 lines 16-57, col. 8 lines 38-63).

Chen et al. and Sonderman et al. are analogous art because they are both related to feed-back and feed-forward methods for controlling semiconductor processing

tools in order to achieve targeted and uniform wafer characteristics and performance values.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chen et al. with Sonderman et al. since Sonderman et al. teaches that wafer metrology data collected at certain processing tools (e.g., a deposition tool and an etch tool) can be used to feedback compensate the respective processing tools in order to reduce process non-uniformity across subsequently processed semiconductor wafers (e.g., col. 6 lines 23-27).

Regarding claim 3, Chen et al. in view of Sonderman et al. discloses providing feedback based on the second data to both a lithography process and the etch process, and adjusting at least one of the lithography process and the etch process based on the feedback (e.g., col. 8 line 67 – col. 9 line 3 of Sonderman et al: "The processes performed across the semiconductor wafers **105** may be, but are not limited to, an etch process, CMP process, a photolithography process, an RTA process, and the like", col. 9 lines 34-38 of Sonderman et al.: "The feedback corrections may include adjusting or manipulating one or more process variables to influence the operation of a processing tool **610** on subsequently processed semiconductor wafers 105", *EN: A photolithography tool and an etch tool are included as one of the "processing tools **610**" of Sonderman et al. to which feedback corrections may be applied.*)

It would have been further obvious to one having ordinary skill in the art at the time the invention was made to modify Chen et al. with Sonderman et al. since

Sonderman et al. teaches that wafer metrology data collected at certain processing tools (e.g., an etch tool) can be used to feedback compensate the respective processing tools (including a photolithography tool and an etch tool) in order to reduce process non-uniformity across subsequently processed semiconductor wafers (e.g., col. 6 lines 23-27).

Regarding claims 4, 10, 14, 20, 24, and 30, Chen et al. in view of Sonderman et al. discloses determining a variation in resistance over a plurality of semiconductor wafers (e.g., col. 8 lines 38-63 of Sonderman et al.).

It would have been further obvious to one having ordinary skill in the art at the time the invention was made to modify Chen et al. with Sonderman et al. since Sonderman et al. teaches that determining a variation in resistance over a plurality of semiconductor products (as well as variations in trench depth, sidewall angles, line width, etc.) can be used to help reduce process non-uniformity, properly correct errors detected across the processed wafers, and improve yield prediction and manufacturing planning (e.g., col. 2 lines 51-67).

Regarding claims 8, 18, and 28, Chen et al. in view of Sonderman et al. discloses determining a planarization process to adjust an amount of metal in a trench in order to achieve process uniformity with respect to various data such as trench depth, thickness, and resistance. The determined planarization process includes removal rate and polishing pressure (e.g., col. 6 lines 1-15 of Sonderman et al.).

It would have been further obvious to one having ordinary skill in the art at the time the invention was made to modify Chen et al. with Sonderman et al. since Sonderman et al. teaches that adjusting and manipulating CMP process variables such as rotational speed and polishing arm down force can be used to achieve a desired metal layer thickness by compensating for a non-uniformity originating in the CMP process itself or in another process, such as a deposition process (e.g., col. 5 line 45 – col. 6 line 15).

Regarding claims 9, 19, and 29, Chen et al. in view of Sonderman et al. discloses measuring an actual wafer resistance (e.g., col. 8 lines 38-63 of Sonderman et al.) and comparing the actual resistance to the target resistance (e.g., col. 5 lines 26-45, col. 6 lines 34-57 et al.).

It would have been further obvious to one having ordinary skill in the art at the time the invention was made to modify Chen et al. with Sonderman et al. since Sonderman et al. teaches that comparing a measured wafer resistance to a target resistance can be used to determine whether uniformity exists across the wafer, or across multiple wafers. Sonderman et al. teaches that process uniformity is important in order to properly correct errors detected across processed wafers, and to improve yield prediction and manufacturing planning (e.g., col. 2 lines 51-67).

Regarding claim 13, Chen et al. in view of Sonderman et al. adjusts the planarization process responsive to the third data that is representative of the second

thickness of the deposition layer and the thickness of the metal (e.g., Fig. 3 #313 of Chen et al.). Chen et al. in view of Sonderman et al. discloses adjusting a deposition process responsive to measured thickness data (e.g., col. 7 lines 30-40, col. 6 lines 16-33, col. 8 lines 38-63 of Sonderman et al.) and adjusting an etch process responsive to measured trench profile data (e.g., col. 7 lines 9-20, col. 6 lines 16-33, col. 8 lines 38-63 of Sonderman et al.).

It would have been further obvious to one having ordinary skill in the art at the time the invention was made to modify Chen et al. with Sonderman et al. since Sonderman et al. teaches that wafer metrology data collected at certain processing tools (e.g., a deposition tool and an etch tool) can be used to feedback compensate the respective processing tools in order to reduce process non-uniformity across subsequently processed semiconductor wafers (e.g., col. 6 lines 23-27).

4. Claim 6, 16, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. in view of Sonderman et al. as applied to claims 1, 11, and 21 above, and further in view of Berghaus et al. US 6,244,103. Chen et al. in view of Sonderman et al. discloses that the plurality of measurements characterizing the trench profile includes at least depth and trench width, or critical dimension (e.g., col. 3 line 62 – col. 4 line 23 of Chen et al.).

Chen et al. in view of Sonderman et al. fails to explicitly disclose that the trench width measurements specifically include a top critical dimension, a bottom critical dimension, and at least one critical dimension along a sidewall of the at least one

trench. The trench depicted in Fig. 2 of Chen et al. is a rectangular trench with a uniform width along the depth of the trench. So in this particular example it would not be necessary to separately measure a top trench width and a bottom trench width since the widths would be the same due to the rectangular nature of the trench. The area of the trench of Chen et al. is represented by the WT term in the equation for calculating the resistance of the trench line (col. 4 lines 46-50), where W is the width of the trench and T is the depth of the trench.

However, trapezoidal-shaped trenches are well known in the art. And it is well known that in order to calculate the area of a trapezoidal-shaped trench one would need to know the values of the top critical dimension and the bottom critical dimension, since the area of a trapezoid is defined as ½ * (top width + bottom width) * height. And, as noted above, Chen et al. already provides a teaching for determining the area of a rectangular-shaped trench.

Berghaus et al. discloses that trapezoidal-shaped trenches are common. Berghaus et al. also discloses a device for determining the entire profile of such a trench, including the top width and bottom width (e.g., col. 1 lines 10-45).

Chen et al. in view of Sonderman et al. and Berghaus et al. are analogous art since they are both concerned with measuring critical dimensions of a trench profile in a semiconductor wafer.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chen et al. in view of Sonderman et al. with Berghaus et al. since Berghaus et al. teaches that sharp trenches with 90° angles are

not always required, and sometimes a process can fall out of specification, resulting in trapezoidal-shaped trenches, which would require a determination of the entire trench profile depending on the situation (col. 1 lines 10-45), and since Chen et al. in view of Sonderman et al. already provides a teaching for the desirability of obtaining a cross-sectional area of a trench profile.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan A. Jarrett whose telephone number is (571) 272-3742. The examiner can normally be reached on 10:00-6:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Jarrett
Examiner
Art Unit 2125

11/14/05
RAJ

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100